Exhibit 4

iSmartgate Cameras (see product list at end of chart for models) Infringement of the '790 patent	
Claim 1	**Evidence**
1. An interface for receiving data from an image sensor having an imaging array and a clock generator for transfer to a processor system comprising:	The iSmartgate camera provides an interface for receiving data from an image sensor having an imaging array and a clock generator for transfer to a processor system. For example, the iSmartgate camera includes a processor that processes image data. The iSmartgate camera includes interface circuitry that receives image data from an image capturing system, which includes a CMOS image sensor, and transfers the image data to the processor. The interface circuitry thereby enables the transfer of image data between the image capturing system, which runs in a pixel clock domain, and the image processor, which runs in a processor clock domain.
a memory for storing imaging array data and clocking signals at a rate determined by the clocking signals;	The iSmartgate camera provides a memory for storing imaging array data and clocking signals at a rate determined by the clocking signals. For example, the interface circuitry of the iSmartgate camera includes a buffer module that stores the image data that is received from the image capturing system. The buffer module has control and clock signal inputs. The buffer module clocks its internal and external signals at a rate that is determined by the input clock signals. This enables the buffer module to store the image data at a rate that is in accordance with the pixel clock domain of the image capturing system.
a signal generator for generating a signal for transmission to the processor system in response to the quantity of data in the memory; and	The iSmartgate camera provides a signal generator for generating a signal for transmission to the processor system in response to the quantity of data in the memory. For example, the interface circuitry of the iSmartgate camera includes interface functionality that generates a signal when the buffer module has image data that is ready for

	transmission to the processor. The signal indicates that the buffer module has a frame or sub-frame of image data for the processor.
a circuit for controlling the transfer of the data from the memory at a rate determined by the processor system.	The iSmartgate camera provides a circuit for controlling the transfer of the data from the memory at a rate determined by the processor system. For example, the interface circuitry of the iSmartgate camera includes timing and control functionality that controls the transfer of image data from the buffer module to the processor. The timing and control functionality enables the image data to be transferred at a rate determined by the processor. This enables the processor to acquire the image data at a rate that is in accordance with the processor clock domain.

Product List

iSmartgate Doorbell
iSmartgate Indoor Camera
iSmartgate Outdoor Camera

References

[1] iSmartgate – Compare Surveillance Products
https://ismartgate.com/compare-ismartgate-surveillance-products/

[2] iSmartgate – Doorbell
https://ismartgate.com/ismartgate-smart-video-doorbell-wired/

[3] Amazon: iSmartgate Indoor Camera
https://www.amazon.ca/ismartgate-Indoor-Camera-Garage-Surveillance/dp/B08BCLG9WS/ref=sr_1_7?keywords=ISMARTGATE&qid=1638400031&sr=8-7

[4] Amazon: iSmartgate Outdoor Camera
https://www.amazon.ca/ismartgate-Outdoor-Camera-1080p-Surveillance/dp/B08DV9ST4B/ref=sr_1_8?keywords=ISMARTGATE&qid=1638400031&sr=8-8